CV date:	**October 10, 2019**

Part A. PERSONAL INFORMATION

First and Family name	ANTONIO JOSE ACOSTA JIMENEZ		
Social Security, Passport, ID number	28885593P	Age	52
Researcher codes	WoS Researcher ID *(*)*	M-9614-2018	
	SCOPUS Author ID*(*)*		
	Open Researcher and Contributor ID (ORCID) **	0000-0002-7934-9162	

(*) At least one of these is mandatory
(**) Mandatory

A.1. Current position

Name of University/Institution	Universidad de Sevilla			
Department	Electrónica y Electromagnetismo			
Address and Country	Avda. Reina Mercedes s/n, Sevilla, España			
Phone number	954466666	E-mail	acojim@us.es	
Current position	Full Professor (Catedrático de Univ)		From	2011
Key words	Power, timing and noise in CMOS technologies; high-performance digital and mixed-signal ASICs design; crypto-hardware; control, artificial vision and crypto-biometric embedded applications			

A.2. Education

PhD	University	Year
MsC Electronic Physics	SEVILLA	1989
PhD Physics	SEVILLA	1995

A.3. JCR articles, h Index, thesis supervised…

- Recognized 6-year Research Periods *(Sexenios de investigación): 4 (1990-95, 1996-2001, 2002-07, 2008-13).* 5th expected *2014-19.*
- Supervised PhD Thesis: 5 (4 in last 10 years)
- Cited by: 1367 *(Google Scholar)*
- Cites/year (last 5 years): 106 *(Google Scholar)*
- JCR total: 29 (12 Q1)
- h-Index: 17 *(Google Scholar)*
- Other indicators: Index i10: 29 *(Google Scholar), 13 (last 5 years)*

Part B. CV SUMMARY *(max. 3500 characters, including spaces)*

Teaching Activities

Teaching in Universitary Studies since 1990. Coordinator of subjects and supervisor of Graduate (15) and Master Thesis (13). Participant (7) and IP (4) in teaching innovation projects. Assistant, speaker (7) and reviewer in Teaching Conferences (TAEE, IEEE Educon) and lecturer in University Extension courses.
Launch (secretary of the COA, editor of the Verification Report) of the Master in Microelectronics, pioneer title of on-line learning at the Univ. of Seville, of which he has been coordinator in 2011-16.
Prizes for teaching excellence (93/94 and 05/06), with 5 recognized 5-year teaching periods.

Scientific Activities

Affiliated to the Instituto de Microelectrónica de Sevilla, and to the TIC-180 group (Andalusian Research Plan) "Design of Digital and Mixed-Signal Integrated Circuits", he has led (7) and participated (25) in R+D+i Projects in the area of Microelectronics, with applications to cryptography, communications, control, artificial vision, etc, focused on the design, integration and test of ASICs and high-performance mixed-signal systems. He collaborates regularly with national and international research teams.

He is co-author of 2 books, 2 book chapters and 29 papers in high quality indexed journals in his area (TCAS, JSSC, TCOM, TNN, IJCTA, EL, etc).
He has 121 publications in very prestigious international conferences (DATE, ESSCIRC, ISCAS, PATMOS, ECCTD, ICECS, etc), to which he habitually attends as a speaker or chair session (some have acceptance rate below 25%).
He has led (2) and participated (9) in contracts with industry. He has one patent with a PCT extension that is being exploited. He has supervised 5 doctoral Thesis.
He is Associate Editor of: Integration (Elsevier), Int. J. of Circ. Theory and Apps. (Wiley), J. of Low Power Electronics (ASPBs) and IEEE Trans. on Circuits and Systems-II.
With Prof. T. Addabbo (U. Siena) he has edited the special issue "Secure lightweight cryptohardware" in Int. J. of Circ. Theory and Apps, February 2017.
He has participated in the organization of PATMOS02 (General Chair), DCIS07, ECCTD07, ETS09, ESSCIRC10, Track Chair of ICECS08,10, ECCTD07,13. He has been a panelist at DTIS07, FEDRF17 and guest lecturer at ESSA14. He has been a member of DATE, FTFC, GLSVLSI, PECCS Program Committees. He has organized special sessions at ECCTD07 and ICM10. He is a reviewer of conferences and journals (more than 700 reviews).

Management Activities
Secretary (4/09-6/12) and Director (6/12-3/16) of the Dept. of Electronics and Electromagnetism; Vicedean of Academic Affairs (3/16-5/17) and Dean (5/17-follows), Fac. of Physics; Member of Research Commission (6/19-follows) and Elected Member of the Cloister Board, all in the Univ. of Seville (9/1/18-follows)
Deputy of the subarea "Electronics" of the TEC area of the ANEP, in 2009-13, managing expert evaluations in national and regional calls. Representative in the evaluation pannels of the National Plan in the TEC Area and in the RyC and JdC Contract Commissions.
Member of the Panel of Experts 2015 of the National Plan in the TEC, Challenges and Excellence Area. Member of the 2011 Evaluation Panel of INTA's Strategic Plan. Member of the Steering Committee of PATMOS since 2002.

Dissemination Activities
IP of 3 funded scientific dissemination projects, participating in talks in different forums, Researchers' Night, etc. He has written the book "La Nanotecnología", from the series "Un Paseo por el Cosmos" (RBA Editores, 2016).

Part C. RELEVANT MERITS (since 1/1/2009)

C.1. Publications (including books)

Journals (+2 submitted for publication to ACM JETC and IEEE TETC in the topic of SIRoT):

1. Tena E., **Acosta, A.J.**, Logic minimization and wide fan-in issues in DPL-based cryptocircuits against power analysis attacks. Int. J. Circ T. Appl. 47(2), 238-253, 2019.
2. **Acosta, A.J.**, Addabbo, Tommaso, Tena, E., Embedded electronic circuits for cryptography, hardware security and true random number generation: an overview. Int. J. Circ. Theor Appl, 45-2: 145-169, 2017.
3. **Acosta, A.J.**, Tena, E., Jiménez, C.J., Mora, J.M., “Power and energy issues on lightweight cryptography”, J.of Low Power Electronics, 13(3), 326-337, 2017.
4. Brox, P.; Martínez, M.C.; Tena, E.; Baturone, I.; **Acosta, A.J.**, Application specific integrated circuit solution for multi- input multi-output piecewise-affine functions. Int. J. on Circuit Theory and Appl, 44: 4-20, 2016
5. Tena, E.; Castro, J.; **Acosta, A.J.**, A Methodology for Optimized Design of Secure Differential Logic Gates for DPA Resistant Circuits. IEEE Journal on Emerging and Selected Topics in Circuits and Systems. 4: 203-215, 2014
6. Brox, P.; Castro, J.; Martínez, M.C.; Tena, E.; Jiménez, C.J.; Baturone, I.; **Acosta, A.J.**, A Programmable and Configurable ASIC to Generate Piecewise-Affine Functions Defined over General Partitions. IEEE Trans. on Circuits and Systems-I. 60-12: 3182-3194, 2013
7. Camuñas, L.; Zamarreño, C.; Linares, A.; **Acosta, A.J.**; Serrano, T.; Linares, B., An

event-driven multi-kernel convolution processor module for event-driven vision sensors, IEEE J. of Solid-State Circuits 47 (2), 504-517, 2011.

8. Camuñas, L.; **Acosta, A.J.**; Zamarreño, C.; Serrano, T.; Linares, B., A 32x32 Pixel Convolution Processor Chip for Address Event Vision Sensors with 155 ns Event Latency and 20 Meps Throughput, IEEE Trans. on Circuits and Systems I. 58 (4), 777-790, 2010

9. Serrano, R.; Oster, M.; Lichtsteiner, P.; Linares, A.; Paz, R.; Gómez, F.; Camuñas, L.; Berner, R.; Rivas, M.; Delbruck, T.; Liu, S-C.; Douglas, R.; Hafliger, P.; Jiménez, G.; Civit, A.; Serrano, T.; **Acosta, A.J.**; Linares, B., CAVIAR: A 45k neuron, 5M synapse, 12G connects/s AER hardware sensory–processing–learning–actuating system for high-speed visual object recognition and tracking, IEEE Trans. on Neural Networks 20 (9), 1417-1438, 2009

Conferences (only those related to the topic of SIRoT):

10. Tena, E.; **Acosta, A.J.**, Effect of temperature variation in experimental DPA and DEMA attacks, PATMOS 2018

11. Tena, E.; Delgado, I.; Núñez, J.; **Acosta, A.J.**, Benchmarking of nanometer technologies for DPA-resilient DPL-based cryptocircuits, DCIS 2018

12. Tena, E.; Durán, I.; Canas, S.; **Acosta, A.J.**, Vulnerability Evaluation and Secure Design Methodology of Cryptohardware for ASIC-embedded Secure Applications to Prevent Side-Channel Attacks, DCIS 2016

13. Tena, E.; **Acosta, A.J.**; Núñez, J., Secure Cryptographic Hardware Implementation Issues for High-Performance Applications, PATMOS 2016

14. Tena, E.; Durán, I.; Canas, S.; **Acosta, A.J.**, Vulnerability Evaluation and Secure Design Methodology of Cryptohardware for ASIC-embedded Secure Applications to Prevent Side-Channel Attacks, Poster-TRUDEVICE Workshop, 2016

15. Tena, E.; **Acosta, A.J.**, DPA Vulnerability Analysis on Trivium Stream Cipher Using an Optimized Power Model. IEEE ISCAS 2015, pp. 1846-1849

16. Tena, E.; **Acosta, A.J.**, Optimized DPA attack on Trivium stream cipher using correlation shape distinguishers, DCIS 2015

17. Tena, E.; **Acosta, A.J.**, Design and characterization of cryptohardware for ASIC-embedded secure applications to prevent power analysis attacks. Poster-CHES 2015

18. Tena, E.; Castro, J.; **Acosta, A.J.**, Low-power differential logic gates for DPA resistant circuits, DSD 2014, 671-674

19. Tena, E.; Castro, J.; **Acosta, A.J.**, Design and test of a low-power 90nm XOR/XNOR gate for cryptographic applications, PATMOS 2014

20. Castro, J.; Parra, P.; **Acosta, A.J.**, An improved differential pull-down network logic configuration for DPA resistant circuits, ICM 2010, 311-314

21. Eiroa, S.; Baturone, I.; **Acosta, A.J.**; Dávila, J., Using physical unclonable functions for hardware authentication: A survey, DCIS 2010

C.2. Research projects and grants

1. Integracion y Validacion en Laboratorio de Contramedidas frente a Ataques Laterales en Criptocircuitos Microelectrónicos. Ministerio de Economía y Competitividad, TEC2016-80549-R, 2017-19, IP: **Acosta, A.J.** 86.400€

2. Circuitos Microelectrónicos Seguros Frente a Ataques Laterales. Ministerio de Economía y Competitividad, TEC2013-45534-R. 2014-17. IP: **Acosta, A.J.** 119.400€

3. Circuitos Integrados para Transmisión de Información Especialmente Segura. Ministerio de Ciencia e Innovación, TEC2010-16870. 2011-14. IP: Jiménez, C.J. 106.722€.

4. Model-Based Synthesis of Digital Electronic Circuits for Embedded Control. Comisión Europea IST-VIIPM Nº-248858. 2009-12. IP: **Acosta, A.J.** 450.000€.

5. Diseño Microelectrónico para Autenticación Cripto-Biométrica. Junta de Andalucía TEC2008-3674. 2009-12. IP: Baturone, I.. 439.847€

C.3. Contracts

1. CbDOC: Gestión documental con autenticación segura mediante técnicas Cripto-Biométricas vía hardware, INNPACTO IPT-2012-0695-390000. IP: Baturone, I.. Ministerio de Ciencia e Innovación, 2012-14. 542.811,50€
2. FRAMING: Diseño VLSI de módulo digital serializador (framing) de altas prestaciones para un sensor quad-linear de alta velocidad de 16k píxeles. Industrial contract with Innovaciones Microelectrónicas SL, 2014. IP: Brox, P., 9.000€

C.4. Patents

1. **Acosta, A.J.**; Baturone, I.; Castro, J.; Jimenez, C.J.; Brox, P.; Martínez, M.C. Method for Generating Piecewise-Affine Multivariate Functions with On-Line Computation of the Search Tree and Device for Implementing the Same, P201200608, 2012. Extension PCT/ES2013/000134-WO2013/182717A1. US Patent 20,150,301,555, 2015. Exploited by Canaan R&I

C.5 Invited Conferences

1. **Acosta, A.J.,** Emerging Design Challenges for Complex SoCs, Invited Panelist in 2nd Federative Event on Design for Robustness, July 2017, Thessaloniki (Greece).
2. **Acosta, A.J.,** Low Power and Security Trade-off in Hardware: From True Random Number Generators to DPA Resilience, Energy Secure Systems Architecture Workshop, International Symposium on Circuit Architecture, June 2014, Minneapolis (USA).

C.6 Committees and reviewer

1. Associate Editor of Journals: Integration, the VLSI Journal (Elsevier), Int. J. of Circuit Theory and Applications (Wiley), J. of Low Power Electronics (ASPBs) and IEEE Trans. on Circuits and Systems-II.
2. Member of PATMOS Steering Committee. General Chair of PATMOS 2002
3. Member of Program Committee: DATE, FTFC, GLSVLSI, PECCS and TAEE.
4. Finance Chair of DCIS07, ECCTD07, ETS09 and ESSCIRC10.
5. Track Chair of ICECS08, ICECS10, ICECS15, ECCTD07 and ECCTD13.
6. Organizer of special sessions in ECCTD07 and ICM10.
7. Organizer of special issue “Secure lightweight criptohardware” in Int. J. of Circuit Theory and Applications (Wiley), February 2017.
8. Reviewer of conferences (DATE, ECCTD, ISCAS, ICECS, TAEE, EDUCON, FTFC, GLSVLSI, DCIS, PATMOS) and international journals: IEEE (TCAS-I, -II, TVLSI, JSSC, TCOMP, TSM), EL, JOLPE, Sensors, IJCTA, (more than 700 reviews).

C.7 Research Management

1. Deputy of *Electronics* to coordinator of Area *Electronic Technology and Communications (COM)* of the Agencia Nacional de Evaluación y Prospectiva (ANEP), 03/09-12/13
2. Member of the 2011 Evaluation Panel of Instituto Nacional de Técnica Aeroespacial INTA's Strategic Plan 2011-15
3. Member of the Panel of Experts of the National Plan in the TEC Area, Challenges and Excellence Call, 2014. Ministerio de Economía y Competitividad. Feb. 2015

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C.8 Dissemination

1. Author of scientific book “La Nanotecnología”, from the series “Un Paseo por el Cosmos” (RBA Editores, 2016). ISBN: 978-84-473-8382-5
2. Scientific Advisory of series “Fronteras de la Ciencia”, RBA Editores, 2017.
3. Responsible of 3 Dissemination Projects funded by Univ. of Seville (appearing in media):
   - Evolution of microelectronics through the world of smartphones, 2013. 3000€
   - Do you dare to be a scientist? Approaching microelectronics to students, 2014. 2500€
   - Chips’ world: science and inventiveness in nanoscale, 2015. 2000€
4. Talks on Microelectronics and Nanotechnology in several forums, 2008-18.
5. European Corner. Researchers Night, Seville, 2014.